Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

FEATURES:

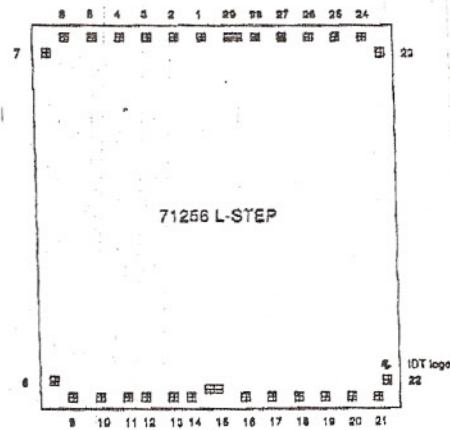
- DIE SIZE: 3360µm x 4480µm
- DIE THICKNESS: 0.020"
- DIE BACKSIDE: Substrate is connected to Vcc, backside should be left floating.
- IDT DIE ATTACH: Silver Epoxy
- IDT WIRE BOND: Au, 0.0013" diameter

PAD COORDINATES

PAD NUMBER	PAD NAME	LOCATION X	LOCATION Y	TYPE
1	A14	-178.0	1970.0	A
2	A12	-349.4	1970.0	A
3	A7	-641.7	1970.0	A
4	A6	-811.2	1970.0	A
5	A5	-1103.4	1970.0	A
6	A4	-1273.0	1970.0	A
7	A3	-1498.1	1849.8	A
8	A2	-1613.7	-1749.3	A
9	A1	-1304.4	-1904.5	A
10	A0	-1136.5	-1904.5	A
11	IO0	-876.0	-1904.5	A
12	IO1	-655.5	-1904.5	A
13	IO2	-419.9	-1904.5	A
14	GND	-228.9	-1956.6	A
15	GND	-60.5	-1904.5	A
17	IO3	182.8	-1904.5	A
18	IO4	406.9	-1904.5	A
19	IO5	642.5	-1904.5	A
20	IO6	866.6	-1904.5	A
21	IO7	1102.1	-1904.5	A
22	$\overline{CS}$	1298.7	-1904.5	A
23	A10	1510.8	-1759.4	A
24	$\overline{OE}$	1495.0	1848.6	A
25	A11	1269.3	1970.0	A
26	A9	1037.4	1970.0	A
27	A8	867.9	1970.0	A
28	A13	575.8	1970.0	A
29	$\overline{WE}$	406.1	1970.0	A
30	VCC	219.6	2018.4	A

All coordinates are in microns and are referenced to the geometric center of the die.

PAD LAYOUT



PAD DIMENSIONS

TYPE	X	Y	UNIT
A	104.0 MIN	104.0 MIN	µm

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads : .004"

APPROVED BY: CB	**DIE SIZE : .036" x .048"**	**DATE: 2/7/01**
MFG: IDT	**THICKNESS: .020"**	**P/N: IDT71256L-20**